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WIDE-RANGE LOW-POWER 1.12PS JITTER DELAY LOCKED LOOP BY A NOVEL LOCK-DETECTION TECHNIQUE

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Abstract

Analog DLLs are formed of a voltage-controlled delay line (VCDL), a phase detector (PD), a charge pump (CP), and a loop filter. Phase Detector is the main component in designing DLLs, in this paper a sensitivity with small dead-zone and reduced number of transistor-based Master-Slave DFF and wide range compatible charge pump is presented. A CMOS delay locked loop design was done and simulated in BSIM3 model of level 49 H-Spice parameters in 180 nm, the supply voltage 1.8V and aim of achieving post-layout simulation and dead zone under 100 ps which resulted in 3.3 mW power consumption and 1.01 ps RMS jitter at 166 MHz. The post-layout results show that in a 130×250 µm2 area, the jitter of DLL in comparison to similar works is reduced as well.

Keywords- Delay Locked Loop, Analog circuit, Phase Detector, Charge Pump, Jitter

Introduction

Delay Locked Loops are widely used in Clock Data Recovery circuits, synthesizers, wireless systems, frequency multiplier and digital applications [1-2]. Synthesizers are used in many communications systems which accurate and stable frequencies are critical in them. When there is no need to multiply frequency, DLLs are a proper choice than PLLs because of their lower jitter, good stability and phase noise. Lock time, power consumption, jitter and phase errors are the main component that could be mentioned in designed DLLs. The DLLs, on the other hand, align the input and delayed clocks. This is done by delaying the input clock after passing it through a delay line and controlling the delay using some mechanism. Once the input clock is delayed a phase detector (PD) compares the phases of the two inputs. Based on PD output value, the delay is adjusted (increased or decreased) until the two phases are aligned [3-4]. Both phase locked loops (PLLs) and delay locked loops (DLLs) are based on the same underlying principle that they try to align the input clock and its delayed version (one period delayed from the input signal) as described in [5-6]. For this purpose, the PLL employs a voltage control oscillator (VCO) block to generate the output by integrating frequencies and comparing the phases of input and output clocks using a phase detector (PD). The PLLs, due to this integrating nature, are used for frequency multiplication applications. The output of the phase detector drives the loop filter which controls the voltage control oscillator thus controlling the alignment. Due to this integrating nature of VCO and filter structures, PLLs are generally higher order systems compared to DLLs [7-8]. Therefore, PLLs have several disadvantages mainly location of zeros inserted to cater for the two poles might be affected due to PVT variations and thus affecting the loop stability [9-10]

During the past few years various analog DLLs have been implemented for the modern high-performance scheduling systems because their phase error is smaller than the digital DLLs.

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However, in the conventional analog DLLs a few tens of clock pulse periods are needed to lock the system due to large initial phase and generating low charge pump current per cycle. Lock time can be decrease by increasing charge pump current and larger voltage ripple on the control node of VCDL that has a significant impact on the performance of clock pulse's jitter. Analog DLLs usually exhibit good noise immunity, better jitter and skew suppression characteristics but they are process sensitive, require larger areas and are quite complex to design as compared to their digital counterparts [11-13].

In [7] a quick lock is presented in DLL with limited jitter characteristics. In the quick lock mechanism, a frequency estimator and an adjustable voltage circuit has been developed that converts the VCDL control node to a voltage level close to the final required amount. Then the DLL output rapidly will be locked by the charge pump on the loop filter. In the limited jitter approach the dual phase frequency detector and an adjustable delay are used. In this section the DLL presented in Figure **1** is designed and implemented in 180 nm CMOS technology. The minimum lock time is measured as 15 clock cycles without reference input to reach the lock mode. Output frequency range of DLL is measured between 50 and 166 MHz, DLL power dissipation is 366 μW at 1.8 V. In this paper in order to accelerate the DLL locking process without increasing the bandwidth of the system loop a flip-flop based phase detector is designed that detects the difference between rising edges of the reference input clock and feedback path in the loop. Then, based on these results the programmable voltage circuit charges or discharges the loop filter continuously. The control voltage V_{ctrl} in VCDL is increased or decreased to reach a voltage corresponding near the final value.

During this time, correct lock detection circuit is embedded in the paths of charging filter capacitors that cuts off charge pump current or connect this path based on the detector performance so that the possibility of incorrect locking could be significantly decreased. In general, it is expected that a DLL output clock at higher frequencies has a lower jitter and the amplitude of control voltage ripple is reduced in VCDL. Ripple may be created by the phase detector's dead zone, input reference jitter, delay loop, losing charge of the capacitor in the loop filter and so on. The proposed structure of DLL is shown in Fig. 1.

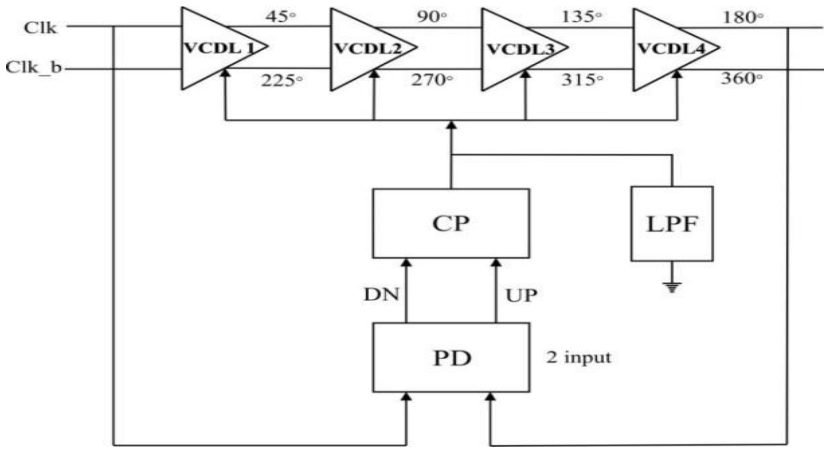

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Figure 1: The proposed DLL structure

In order to adapt the proposed DLL to the high speed performance, an improved phase detector circuit in DFF applications is applied in these circuits that could be proper for a simple edge combiner to synthesize an output clock with N folded input frequency. In the next section, the design considerations for quick lock and methods to limit jitter are presented. The most critical component in the performance of a DLL is a VCDL which directly influence DLL jitter performance and stability. The basic purpose of a VCDL is to delay the input signal by one clock period or equivalently 360°.

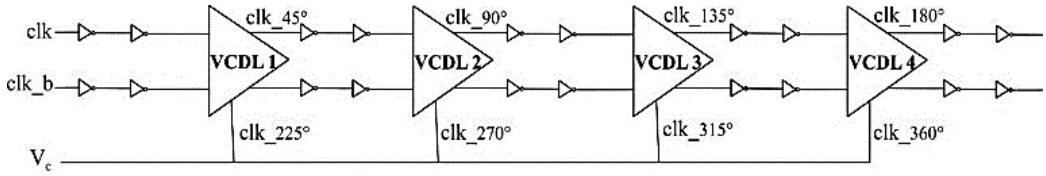

Figure 2: The proposed VCDL structure

A differential structure is applied to realize VCDL to reject common-mode disturbances. To achieve four differential delay cells, the circuit in Fig. 2 is used.

In this diagram since four differential delay cells are used, eight main phases are obtained and two consecutive inverters are used in the outputs to keep the Duty Cycle signal close to 50%. In Fig. 3 the schematics of the improved cells is presented. As discussed in [12], the output jitter of the DLL due to the jitter of delay cells can be proved from the time-domain equations and can be obtained as follows:

$$\sigma^2(\Delta t_N) = \frac{2N}{\left[2-\left(\frac{I_{CP}\times K_{VCDL}}{C_{LF}}\right)\right]} \times \sigma^2(\Delta t_{DS}) \qquad (1)$$

Equation (1) shows the relation of the output jitter of the DLL to the jitter of the delay cells. According to this equation the output jitter is related to I_{CP}, K_{VCDL}, C_{LF} and the number of delay cells in the delay stage (N). As it can see from the relationship, the number of delay cells has a direct relation with the output jitter. So by reducing the number of cells in the delay cells, a lower jitter value can be obtained. The jitter at the output of X_{th} delay cell due to the delay cells' jitter can be expressed as:

$$\sigma^2(\Delta t_X) = \{\frac{(X^2)\times\left(\frac{I_{CP}\times K_{VCDL}}{C_{LF}}\right)}{\left[2-\left(\frac{I_{CP}\times K_{VCDL}}{C_{LF}}\right)\right]} + X\} \times \sigma^2(\Delta t_{DS}) \qquad (2)$$

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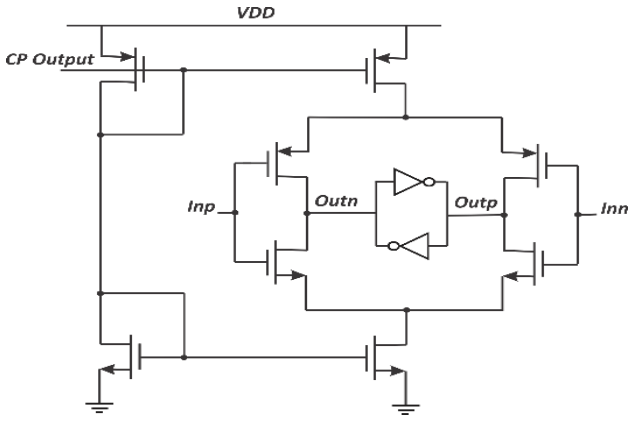

Figure 3: Improved conventional VCDL

Electric current control is done in two directions, it mirrors from the top and bottom of the circuit, and also the inverter is embedded back to back between the outputs of the delay cell. Decreasing the number of delay cell could decrease the jitter and in this design is taken into consideration.

The phase detector is the most important component of a DLL. The purpose of the PD is to detect the difference between its two inputs. One of the inputs to a phase detector is the input clock and the other is a delayed version of this input clock from the delay line or a delayed version of an uncorrelated clock depending on the architecture of the DLL. The simplest phase detector is a single D flip flop (DFF). The DFF is clocked by the input reference clock and detects the difference between the clocks by selecting the Q output of the DFF. If the Q output is low, it means that the output clock (clock signal form the end of digitally controlled delay line) is leading the input reference clock and thus the delay of the delay line must be increased to compensate for the difference in phase until the lock condition is achieved. The proposed phase detector is designed based on Bang- Bang phase detector which its general diagram is shown in Figure 4. This phase detector has two main inputs designed by certain latches as master slave. The main drawback in many previous works was designing PD circuit based on a rising or falling edge of the input pulse.

Figure 4: The general diagram of proposed phase detector

This increases the power consumption in the circuit because the phase detector and charge pump have to wait for reaching the next rising or falling edge. On the other hand, higher number of clock cycles is consumed to adjust the phase error between the UP and DN signals. As a result, to fix these two problems, the new detector design is based on both edges of the input pulse. A much superior PD is based on flip flops as it can detect edges irrelative of the input

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signal's duty cycle. This type of PD can be used for frequency detection along with phase but the setup time may become a limiting factor in achieving good performance results.

To lock the loop quickly it is better to perform PD design such that the UP and DN signals have the minimum glitch value and the best method to achieve this purpose is to choose the

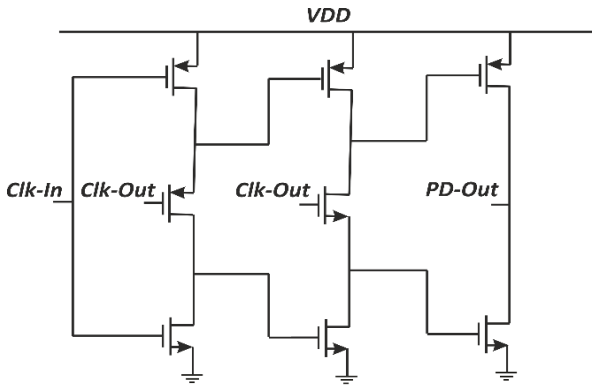

Figure 5. The schematic at the transistor-level structure of each DFF

'V_{DD}' and '0' values for the average value of UP and DN signals. The schematic at the transistor-level structure of each DFF is shown in Figure 5.

In another similar works, evaluation of priority is performed by similar sampling method, meanwhile pulse generator section provides narrow pulses to restrict the time duration of charging in CP that in this design this main part is eliminated as well. This phase detector is capable of detecting the difference between the smaller phases. Hence, phase differences are greater than and equal to 180° if this detection has greater precision. Although this design is simple and effective in most cases but it has several shortcomings. If the setup and hold times are not symmetric this may introduce a regular phase error as lagging and leading decisions based on hold and setup times, respectively.

The phase difference is detected by the PD the difference is sent to the CP which in turn makes changes to the loop filter thus setting the VCDL delay in order to minimize the phase error between the inputs of the PD. The proposed charge pump circuit is shown in Figure 6. Based on the designed circuit, two capacitors lead the output filter in the charge pump. If the signal UP equals "1" and DN equals "0", the capacitor C1 is charged, and if the signal DN equals "1" and UP equals "0", the capacitor C2 is charged. When both inputs equal "0", a leak current flows through both capacitors. Fig. 7 graphically describes the position of the lock detector in the DLL. The increase between the UP and DN current sources leads to increase ripples in the control voltage; leading to higher reference spurs. To solve this problem, a charge pump is designed that is able to detect the correct lock and has no leakage current. Fig. 8 shows its general schematic of proposed lock detector.

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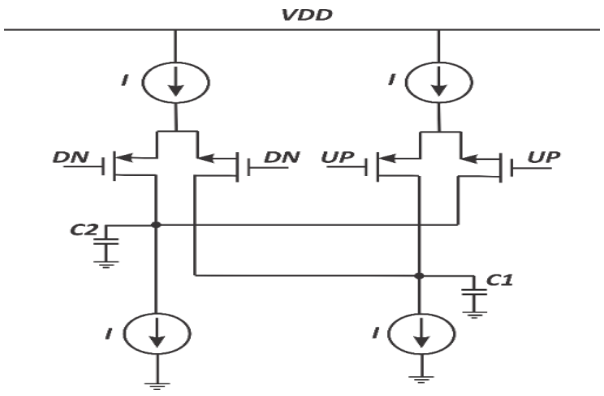

Figure 6: The proposed charge pump circuit

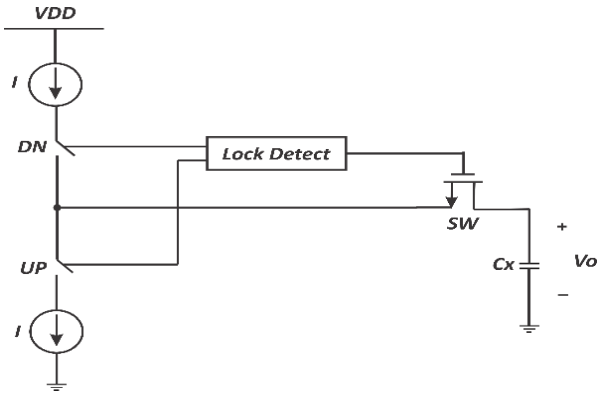

Figure 7: Improved charge pump schematic of the Figure 6

The previous circuit's defect related to current leakage is resolved by the lock detection circuit and when both UP and DN signals are equal "1", the low-pass filter capacitor charging is prevented by applying the lock detect output to the SW switch. Lock detection circuit works when inputs are both "1" or "0", the output will be "0" and applied to the gate of SW switch and cuts it off. The cut-off switch prevents creating current path from the charge pump to the filter capacitor.

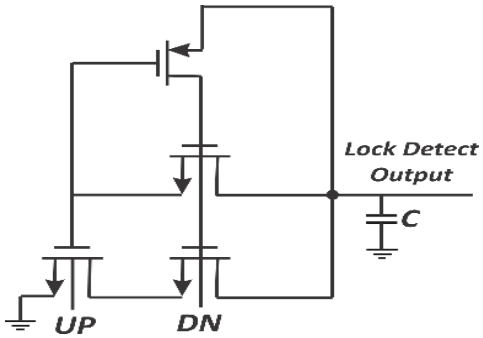

Figure 8: The proposed lock detect circuit

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Simulation Results

First of all, a general simulation is performed in three frequencies of 52, 83 and 166 MHz. Power consumption, jitter, control voltage and the lock time for each frequency is calculated and shown. Finally, the results are shown as tables and diagrams. In order to calculate the output jitter in the frequency of 52 MHz, first the eye diagram of one of the outputs is drawn as shown in Fig. 9. Jitter adjustment is made and the output is selected for one of the rising and falling edges. Afterwards, by choosing the Jitter Measurement and giving the accurate frequency that is expected from the output, the correct amount of jitter is measured.

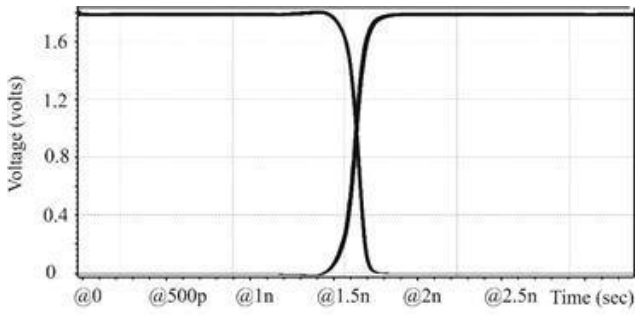

Figure 9: Eye diagram relating to the frequency of 52 MHz

According to the result of this eye diagram, the rising edge of the jitter is calculated in seconds. The jitter diagram of the frequency of 52 MHz without noise is shown in Figure . As it is clear, the effective jitter in this frequency is 1.04 ps.

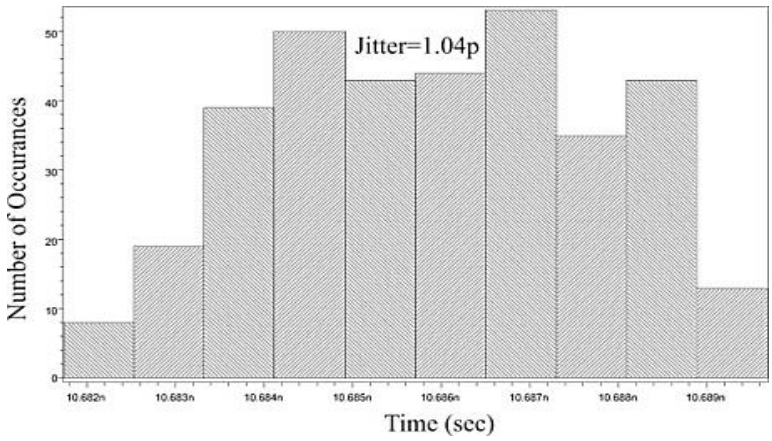

Figure 10: Jitter calculated in the frequency of 52 MHz without noise

Fig. 11 shows the output waveforms before and after the locked loop at the frequency of 120 MHz. In this figure, first diagram is charge pump output, second diagram is main signal and output, third and fourth signals are the signals relating to UP and DN outputs respectively. As it can be seen, the output variations of the charge pump become stable after 105 ns and the

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level of the detector's outputs 'UP' and 'DN' is changed at the same time. Thus the lock time of the DLL is 105 ns at the frequency of 120 MHz. It is clear that the lock time reduces in higher frequencies because the signal's period is reduced and the loop uses less time for locking. The results for the frequency of 166 MHz are provided in the table to be compared to the previous frequencies and with the previous works. All outputs are compared in three considered frequencies and analyzed in the table.

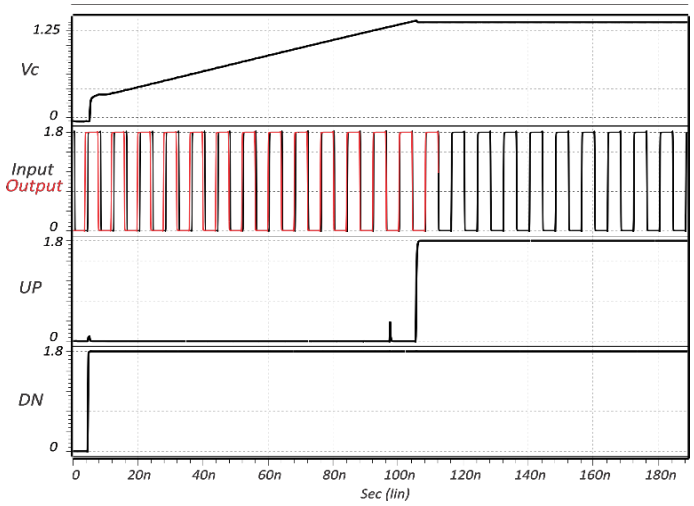

Figure 11: Input and output waveforms before and after the lock at frequency of 120 MHz (post-layout)

It should be noted that all simulations have been performed by applying a 30 mV peak to peak noise related to the power supply. Near the lock time, the CP output will naturally be unstable, depending on the phase and frequency difference between the two inputs of the detector. A non-monotonic behavior will be directly related to the frequency. In other words, the lock time affects the extent of this instability near locks.

Table 1 shows the simulation results in three different frequencies of 52, 83 and 166 MHz. By analyzing the table results, it can be seen that with increasing frequency, lock time and jitter will be reduced as shown in Fig. 12. In contrast, the increase in frequency increases power consumption. Fig. 13 shows power consumption in different frequency. The structure was optimized for low power and low noise. The low CP currents and loop bandwidth are results of this optimization. Obviously, the use of less current will result in more time to charge and discharge the capacitive load, slowing down the response of the structure.

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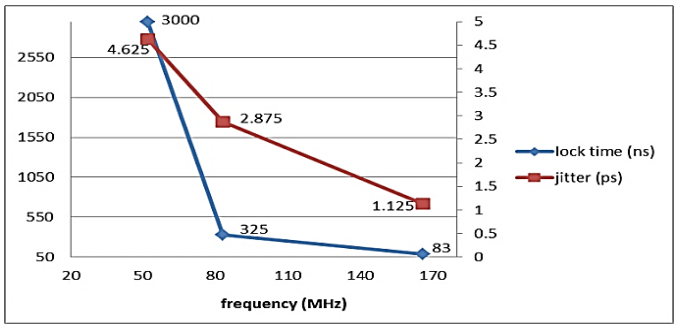

Figure 12: Jitter and lock time comparison diagram with 30 mV P-t-P supply noise

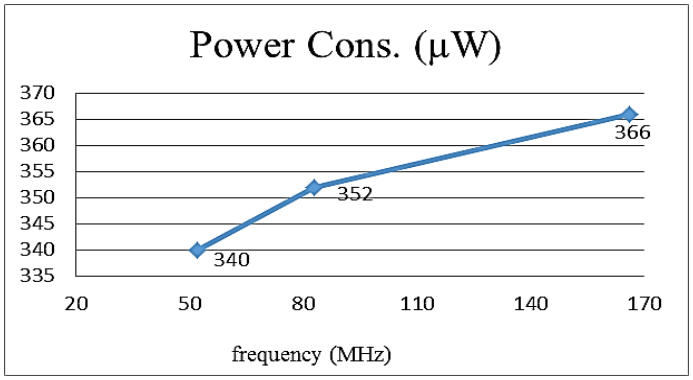

Figure 83: Power Consumption

Table 1. Simulation results

Operating Frequency(MHz) @ 0.18µm	52	83	166
RMS Jitter (ps) for 30mv P-t-P Supply Noise	4.625	2.875	1.125
Power Cons. (µW) @1.8v Supply	340	352	366
Control Voltage (volts)	1.45	1.37	1.18
Lock Time(sec)	3µs	325ns	83ns

Eight output phases in proposed delay locked loop in the frequency of 166 MHz are shown in Figure 9. These output phases include 0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°, and 360° is created by the four differential delay cells in proposed delay locked loop and results are shown in the following.

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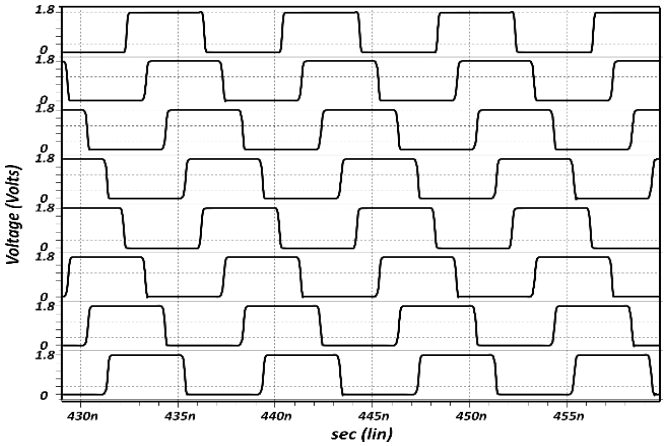

Figure 94: Output phase taken from the delay lock loop for the frequency of 166 MHz (post-layout)

Variations in different corners are also considered in transient behavior. The control voltage is illustrated in Fig. 15 operating frequencies for all process corners. To provide practical conditions of jitter evaluation, noisy supply with the peak-to-peak value of 30 mV is applied on 1.8volt supply voltage. Noise pattern is constructed from a set of sinusoidal voltage sources in series combination with the frequency range of 1MHz to 2.5 GHz. Larger amplitudes are allocated to the multiples of input reference clock as might practically occurs via the substrate coupling. The edge SS has the worst lock mode and the most delay on the frequency of 166 MHz. The simulation in the TT mode is more balanced than other edges.

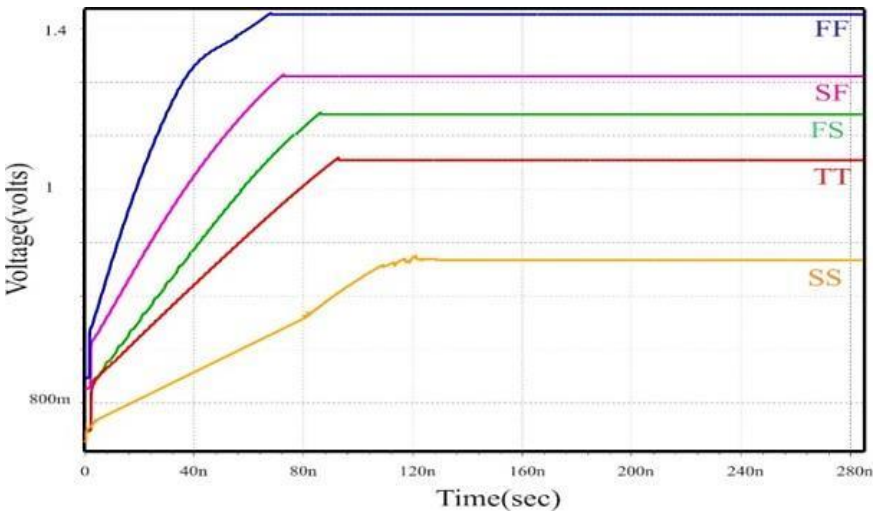

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Figure 15: Post-Layout Simulation of the corners for the frequency of 166MHz

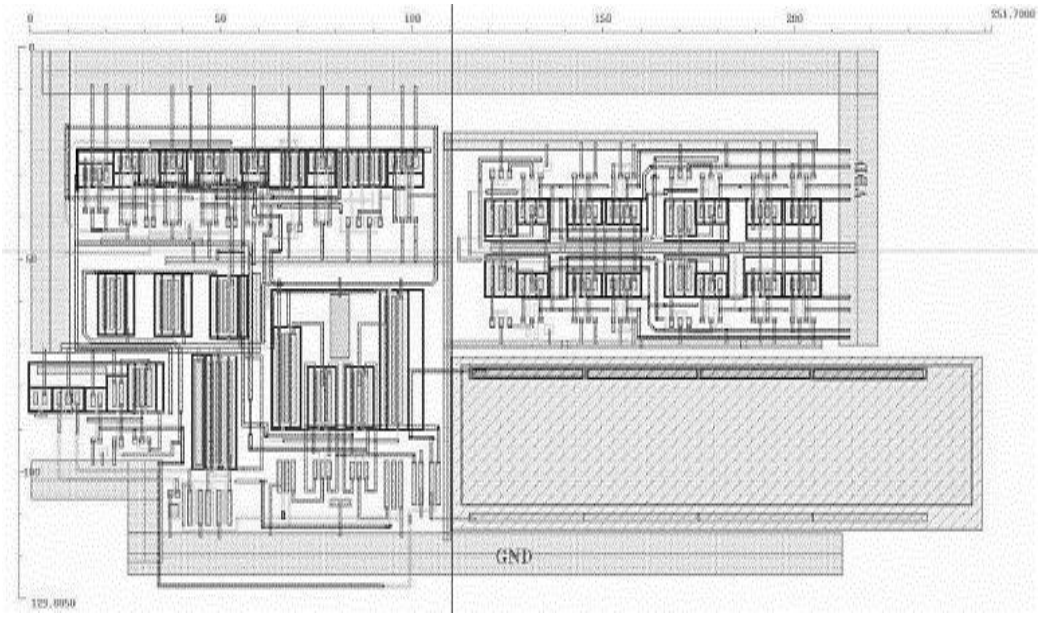

Figure 16: General layout of proposed circuit

Table 2: Results and comparison with other works

	[8]	[9]	[10]	[11]	Proposed
Process (μm)	0.09	0.18	0.045	0.13	0.18
Operating frequency Range (MHz)	6.7-1240	60-1200	500-800	400-800	50-166
Supply (volts)	1.2	1.8	1.1	1.2	1.8
No. Phases	8	N.A	N.A	16	8
RMS Jitter (ps) @ Freq(MHz)	0.4262 @1240	1.63 @1200	1.95 @800	2.3 @800	1.01 @166
Power(mW) @ Freq(MHz)	14 @1240	16.2 @1200	1.32 @800	7.2 @800	3.3 @166

In this paper the simulation of the proposed circuit has been done. Afterwards the layout of this circuit has been implemented in 180 nm CMOS technology. The frequency performance range

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in this case is 50 MHz to 166 MHz. Also the power consumption and the amount of jitter have been a little changed. The layout of the proposed DLL is shown in . As it is clear, the designing is in such a way that uses all the empty spaces as much as possible till less space occupied. The overall dimension of the proposed circuit is 130 × 250 μm^2. Finally the results of this work are provided and compared with some other works in Table 2.

Conclusion

A DLL with a wide range of allowed input duty cycle and a low jitter and low-power with improved phase detector and compatible charge pump is proposed which operates in a wide frequency range from 50MHz to 166MHz. Power consumption would be increased when the operating frequency is reached near to maximum operating frequency. The RMS jitter is also reduced at higher operating frequencies. The results show that by eliminating the pulse-generator circuits in the phase detector circuit, the dead zone was reduced significantly. In order to enhance the general circuit performance interval, a charge pump was used corresponding to the phase detector performance. Series inverters were used to accurately adjust the obtained outputs. The output duty cycles were very close to 50% and it could have eight phases in the frequency interval of mentioned above. In order to further improve the circuit, the method of difference currents may be used for the delay cell to reduce the current flow and to achieve a broadened performance interval without changing the output duty cycles.

References

[1] S. Han, T. Kim and J. Kim, “A 0.1–1.5 GHz all-digital phase inversion delay-locked loop,” in Proc. IEEE Asian Solid State Circuits Conf., 2013, pp. 341–344.

[2] Sofimowloodi, S., Razaghian, F. & Gholami, M. A low-jitter clock multiplier using a simple low-power ECDLL with extra settled delays in VCDL. Analog Integr Circ Sig Process 102, 541–554 (2020).

[3] S. Kazeminia, S.S. Mowloodi, K. Hadidi, A 80-MHz-to-410-MHz 16-phases DLL based on improved dead-zone open-loop phase detector and reduced-gain charge pump. J. Circuits Syst. Comput. 24, 1550001 (2015).

[4] S. R. Al-Araji, E. Salahat, D. Kilani, S. A. Yasin, H. Alkhoja, and J. Aweya, “Adaptive zero-crossing digital phase-locked loop for packet synchronization,” in Proc. IEEE Int. New Circuits Syst. Conf., Jun. 2013, pp. 1–4.

[5] Sofimowloodi, S., Razaghian, F. & Gholami, M. Low-Power High-Frequency Phase Frequency Detector for Minimal Blind-Zone Phase-Locked Loops. Circuits Syst Signal Process (2018).

[6] Kao, Shao-ku. "A delay-locked loop with self-calibration circuit for reducing phase error." Microelectronics Journal 44.8 (2013): 663-669.

[7] M. Gholami, Phase detector with minimal blind zone and reset time for GSamples/s DLLs. Circuits Syst Signal Process. 36, 3549–3563 (2017).

[8] M. H. Hsieh et al., “A 6.7 MHz to 1.24 GHz 0.0318 mm2 fast-locking all-digital DLL using phase- racing delay unit in 90 nm CMOS,” IEEE J. Solid-State Circuits, vol. 51, no. 2, pp. 412–427, Feb. 2016.

[9] C.-Y. Yao, Y.-H. Ho, Y.-Y. Chiu, and R.-J. Yang, “Designing a SAR based all-digital delay-locked loop with constant acquisition cycles using a resettable delay line,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 23, no. 3, pp. 567–574, Mar. 2015.

The Seybold Report
ISSN 1533-9211
DOI 10.5281/zenodo.7262773

[10] D. H. Jung, K. Ryu, J.-H. Park, and S.-O. Jung, "All-digital 90° phase-shift DLL with dithering jitter suppression scheme," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 3, pp. 1015–1024, Mar. 2016.

[11] K. Ryu, D.-H. Jung, and S.-O. Jung, "Process-variation-calibrated multiphase delay locked loop with a loop-embedded duty cycle corrector," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 1, pp. 1–5, Jan. 2014.

[12] Mohammad Gholami, Gholamreza Ardeshir. "Analysis of DLL Jitter due to voltage- controlled Delay Line" Circuits, Systems, and Signal Processing, 11 April 2013.

[13] Estebsari M, Gholami M, Ghahramanpour MJ. A wide frequency range delay line for fast-locking and low power delay-locked-loops. Analog Integr Circuits Signal Process. 2017; 90(2):427-434