The Seybold REPORT

ISSN 1533-9211

DOI: 10.5281/zenodo.13283086

PERFORMANCE ANALYSIS OF A 7nm FinFET DEVICE USING High-k (HK) DIELECTRIC OXIDE MATERIAL WITH k = 24, 25, 30 AND GaAs AS METAL GATE (MG) MATERIAL

MOHAMMED ABDUL MUQEET *

Research Scholar, Department of Electronics and Communication Engineering, University College of Engineering, Acharya Nagarjuna University, Andhra Pradesh, Guntur, India.
* Corresponding Author Email: abdulmqt19@gmail.com

TUMMALA RANGA BABU

Department of Electronics and Communication Engineering, R.V.R. & J.C. College of Engineering, Guntur, Andhra Pradesh, India. Email: trangababu@rvrjc.ac.in

Abstract

The article investigates the benefits of scaling Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and emphasizes FinFETs advantages over planar MOSFETs, notably in terms of decreasing short-channel effects (SCEs) and boosting device performance. High-k (HK) dielectric oxide materials employed include Hafnium Oxide (HfO_2), Lanthanum Oxide (La_2O_3), and Lanthanum Aluminum Oxide ($LaAlO_3$). These materials have excellent features such as high dielectric constant, better permittivity and increased electron mobility. The key performance measures investigated include saturation drain current (I_d(sat)), electric field distribution, electro-static potential, energy densities, threshold voltage (V_{th}), transconductance (g_m), Drain Induced Barrier Lowering (DIBL) and subthreshold swing (SS). The findings show that using HK dielectrics with a GaAs metal gate improves device performance substantially, especially in terms of electric charge densities, electric field distribution, temperature sensitivity, see beck coefficient and overall device stability and efficiency. The study suggests that high-k dielectric materials are more suitable for advanced nanoelectronics applications than SiO_2.

Keywords: Saturation Drain Current, Electric Field Distribution, Electro-Static Potential, Energy Densities, Threshold Voltage, Transconductance, Drain Induced Barrier Lowering and Subthreshold Swing.

I. INTRODUCTION

The process of scaling Metal Oxide Semiconductor Field Effect Transistors (MOSFET) has provided a large increase in device density per wafer, subsequently leading in a notable drop in the cost per chip [1]. In addition to facilitating the widespread integration of electronic components, the transition from the era of microelectronics to the emerging era of nanoelectronics will also enable the miniaturization of these components and a reduction in their costs to the extent that they can be incorporated into virtually any object, including products that are wearable and dissolvable [2]–[4]. In addition, the reduction in the size of transistors that occurs as a consequence of scaling the device brings about other benefits. To be more specific, the decrease in the size of interconnects reduces the distance that electrons have to travel, which in turn reduces the resistance that they encounter along the journey. There is a direct correlation between this decrease in resistance and improvements in circuit delays, power consumption, and speed [5]. As a general rule, a MOSFET device is considered to be in a state of shortness when the channel length reaches a size that is equivalent to the depletion-layer

The Seybold REPORT

ISSN 1533-9211

DOI: 10.5281/zenodo.13283086

widths of both the source and the drain. This results in the appearance of what is popularly known as short-channel effects (SCEs). In order to prioritize the effective gate length, it is a principle that is generally acknowledged. This concept requires that the effective gate length be greater than the thickness of the dielectric oxide zone by a factor of at least forty (Lg>40*Tox) [6], [7]. In the nanoscale realm, this would result in further limits being placed on the scalability of the system.

Researchers have developed an approach that involves the employment of high-k Dielectric (HK) oxide materials in combination with metal gate (MG) for advanced / non-planar field-effect transistor (FET) architectures such as FinFETs [8], [9]. This strategy was developed in order to alleviate the inherent restriction that has been identified. The covalent bonds that are shown by elements that belong to group III-IV is, without a doubt, fascinating components of the two-dimensional (2D) materials class [10]. The HK elements, namely Hafnium Oxide (HfO_2), Lanthanum Oxide (La_2O_3), and Lanthanum Aluminum Oxide ($LaAlO_3$), each having a dielectric constant of k=24, 25 and 30 respectively, are characterized by exceptional properties, including smooth surfaces, the absence of dangling bonds, and an atomic thinness that is genuinely astounding [11], [12]. As a consequence of this, electronics that are based on these materials display significant electron mobility and large ON/OFF current ratios [13], [14]. In the context of HK dielectrics, which display increased oxygen diffusivities at elevated temperatures, it is realistic to predict the occurrence of fast oxygen diffusion through the oxides when exposed to annealing processes that are accompanied by an excessive quantity of oxygen that is present [14], [15]. Each of the dielectric kappa (k) materials is shown in Table-2, along with their associated energy band gaps. The device's performance is significantly enhanced when high-k dielectric materials are used in its construction. An example of this would be the generation of a gate capacitance (C_g) and ON-current (I_{ON}) that are comparable when a 2nm film of SiO_2 is used in conjunction with a 12nm film of HfO_2 gate material.

The evaluation of a HK dielectric as a suitable alternative for SiO_2 is critically dependent on the mobility assessment, which acts as a fundamental component in the evaluation process. A number of transistor measures are significantly impacted by the technique that was just described. These metrics include, but are not limited to, saturation drain current (I_d(sat)), Electric field distribution, threshold voltage (V_{th}), transconductance (g_m), Drain Induced Barrier Lowering (DIBL), and subthreshold swing (SS). There are a number of benefits that may be obtained via the use of FinFET technology in conjunction with HK-MG. The most important of these benefits is the lowering of the subthreshold swing, which can be achieved while simultaneously maintaining a low level of DIBL effect [16]–[19].

II. METHODS & MATERIALS

To provide a theoretical foundation for FinFETs, electrostatic knowledge must be combined with quantum mechanics effects, particularly in the setting of ultra-scaled devices. The multi-gate construction of FinFETs provides a significant advantage over standard planar MOSFETs. This arrangement provides good gate control over the channel, leading in a considerable decrease in leakage current and improved switch-on and switch-off performance. By enclosing

The Seybold Report
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

the gate on three sides of the fin, the electric field is equally distributed over the channel, increasing scalability without sacrificing power consumption or performance. The device driving current (I_d(sat)) and threshold voltage (V_{th}) are heavily dependent on its height (H_{fin}), width (t_{fin}), and HK-MG materials. The fin's aspect ratio rises as technology advances, resulting in enhanced electrostatic control. However, this advancement has also presented issues in maintaining industrial regularity and reducing variability. Furthermore, the mechanical stress generated by the fin structure may be employed to increase carrier mobility via strain engineering.

The DG-FinFET employs a dual-gate construction, with gates located on the sides of a fin-shaped silicon device. The conceptual framework of all such critical aspects is explored, and the device characteristics are represented in Table-1 for the 7nm technology node. A FinFET device is symmetrical, and it is hard to distinguish between them without the bias applied. Shallow trench isolations (STI), are used in bulk FinFET device design to isolate several devices generated on the same substrate. Figure-1 depicts the revolutionary three-dimensional (3D) structure of bulk FinFET (Fin Field-Effect Transistor) devices, which overcomes the drawbacks of ordinary planar MOSFET and represents a significant advancement in semiconductor technology. Additional technical aspects for bulk-FinFETs include field oxide or thickness (T_{ox}), which is utilized to separate adjacent devices. FinFETs are manufactured using the same technology as CMOS. Nonetheless, there are certain stages or modules in the process that need further limitations and optimization. For example, such criteria include maintaining the fin critical dimension (CD) and H_{fin}.

Table 1: 7nm FinFET Device Parameters

Parameter	Value
Channel Length (L)	15nm
Channel Width (W)	7nm
Channel Height (H)	18nm
Oxide Thickness or thickness of the fin (t_{ox} / t_{fin})	6.5nm
Gate Length (L_g)	30nm
Source or Drain Length (L_s or L_d)	2nm
Source of Drain Overlap to Gate	0.2nnm
Source or Drain Doping concentration	3.00E+26 cm-3
Channel Doping	2.86.00E+25 cm-3
Gate Voltage (V_g)	0.7V
Temperature	300k
Drain Voltage (V_d)	0.01 – 0.69V
Oxide Material	Silicon Dioxide (SiO_2) Hafnium Oxide (HfO_2) Lanthanum Oxide (La_2O_3) Lanthanum Aluminium Oxide ($LaAlO_3$)
Gate Material	Gallium Arsenide (GaAs)

The Seybold Report
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

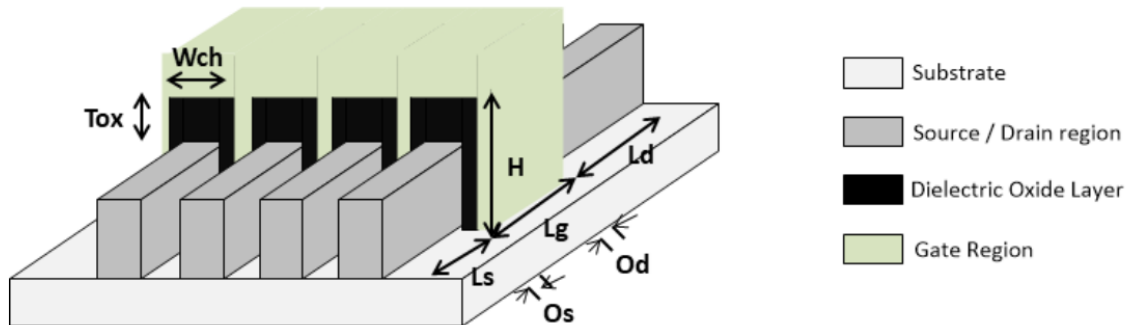

Figure 1: 3D FinFET Structure

The fin-like structure protrudes vertically from the substrate and conducts current, distinguishing FinFETs from conventional MOSFETs. Compared to planar structure, wrapping the gate electrode around the fin increases electrostatic control. This configuration which covers three sides of the fin and dramatically affects the channel.

Height (H_{fin}), breadth (t_{fin}), and length (L_g) are the fin's most important measurements since they affect electrical properties. Less fin width gives the gate better channel control. The fin's height increases channel area, which may boost driving current. These fins have strongly doped source and drain portions on either side for carrier injection into the channel. The gate-to-source voltage (V_{gs}) and drain-to-source voltage (V_{ds}) determine FinFET modes.

Due to minority carrier dispersion, only a limited amount of leakage current occurs in the subthreshold region ($V_{gs} < V_{th}$). This mode is essential for low-power, low-leakage applications. When $V_{gs} > V_{th}$ and V_{ds} is low, the device enters the linear (or ohmic) region, where current increases linearly with V_{ds}.

Analog applications may profit from this voltage-controlled variable resistor-like behavior. The gadget becomes saturation (or active) when V_{ds} rises. Current is essentially steady as voltage increases in this region. In digital switching applications, this mode offers a stable current for dependable operation.

The threshold voltage (V_{th}) is crucial to FinFET functioning. This impacts the gate voltage needed to establish a source-drain conductive channel. Besides gate material, doping concentrations, and fin dimensions, several other parameters affect this threshold. FinFETs offset SCEs better than planar MOSFETs. FinFET functioning requires regulating self-heating effects (SHE), which are caused by the thin fin's higher current density.

Thermal management is important because self-heating may affect device performance and dependability. Despite its drawbacks, FinFETs have several benefits. The wrap-around gate design improves electrostatic control, reducing leakage currents and improving performance. FinFETs' scalability enhances Moore's Law, enabling smaller, more efficient, and more powerful transistors.

The Seybold Report
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

Table 2: High-k Dielectric Materials

HK Material	Dielectric (k) kappa-value	Permittivity, ε (F/m)	Band Gap , Eg (eV)
Silicon Dioxide (SiO_2)	3.9	7.5	9
Silicon Nitride (Si_3N_4)	7.5	8.5	5.3
Aluminium Oxide (Al_2O_3)	9	10	7
Hafnium Silicide ($HfSiO_2$)	11	10.8	6
Lutetium Oxide (Lu_2O_3)	15.95	12.4	5.5
Lanthanum Zirconate ($La_2Zr_2O_7$)	16.4	18	4
Cerium Oxide (CeO_2)	20	23	6
Zirconium Oxide (ZrO_2)	23	23	6
Hafnium Oxide (HfO_2)	24	25	6
Lanthanum Oxide (La_2O_3)	25	26	6
Lanthanum Aluminium Oxide ($LaAlO_3$)	30	29	5.6
Hafnium Titanium Oxide ($HfTiO_2$)	60	43	5.7
Manganese Dioxide (MnO2)	101.5	85	3.05
Niobium Oxide (Nb_2O_5)	200	169	-

Table 3: Metal Gate (MG) Materials

Parameters / Metal Gate (MG) Material	Si	Ge	GaAs	InN	GaN
Dielectric Constant	11.7	16.2	12.9	15.3	10.6
Bandgap eV	1.12	0.8	1.42	1.97	3.28
Electron Affinity, eV	4.05	4	4.07	4.7	1.84
Gate Work Function, eV	4.6	4.8	4.69	4.7	4.1
Electron Effective Mass, Kg	0.19	0.22	0.063	0.12	0.13
Density, kg/m^3	1.18	5.32	5.32	6.81	-
Electron Mobility,$m^2/V\cdot s$	1400	4000	9000	250	1500
Hole Effective Mass, kg	0.16	0.34	0.082	0.27	1.4
Hole Mobility, $m^2/V\cdot s$	450	2000	100	50	40

In advanced MOS technology, the high-k dielectric is employed with metal gates. This is due to the high dielectric constant and broad bandgap of high-k dielectrics. HfO_2, a high-k dielectric with a permittivity of 25 and a bandgap of 5.7 eV, is usually used as the gate dielectric for n- and p-FinFET devices. HfO_2 has a high heat of synthesis, good thermal and chemical stability on silicon, and a high barrier height at silicon surfaces. The leakage current in HfO_2 dielectric films is much lower than that in SiO_2 films with the same equivalent oxide thickness (EOT) for operating voltages between 1 and 1.5 micro-volts (μV). To incorporate HfO_2 for sub-22 nm FinFETs, the thermal instability of the HfO_2/Si contact is one of the biggest challenges. HfO_2/Si is thermodynamically stable in principle, but an inevitable SiO2 interlayer occurs between the HfO2 and the silicon substrate. Table-2 and Table-3 shows the high-k dielectric and metal gate technology parameters. The low carrier density of polysilicon limits its depletion depth to a few angstroms. Despite its low carrier density, polysilicon possesses mild metallic properties. A good-grade metal has a greater carrier density and a lesser depletion depth of 0.5 Å, according to the comparison. Poly-Si may be replaced with a common metal to lessen depletion damage.

ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

III. RESULTS AND DISCUSSIONS

The modeling of FinFET device architectures using HK-MG materials is an important step toward understanding their performance and future applications. This section describes the methods and results of modeling FinFET devices employing high-k dielectrics like HfO_2, La_2O_3, and $LaAlO_3$ in contrast to standard SiO_2, as well as metal gate materials like GaAs.

3.1 Electric Charge Densities

The number of holes (positively charged carriers) contained inside a semiconductor material is referred to as its charge density. A higher hole charge density suggests more positive charge carriers, which improves the conductivity of p-type semiconductors. In contrast, a fall indicates a smaller concentration of holes, which reduces the materials conductivity. Devices such as p-type transistors and diodes need a high hole density to ensure effective hole conduction. Materials having a limited number of holes may be appropriate for applications needing high resistivity. Electron charge density quantifies the amount of electrons (negatively charged particles) in a semiconductor material. An increase in electron charge density implies a greater number of negative charge carriers, increasing the conductivity of n-type semiconductors. In contrast, a decrease in electron charge density implies a drop in the number of electrons, lowering the material's conductivity. High electron density is required for n-type transistors and other electronic devices that depend on efficient electron conduction, but low electron density materials may be used in applications that need low conductivity.

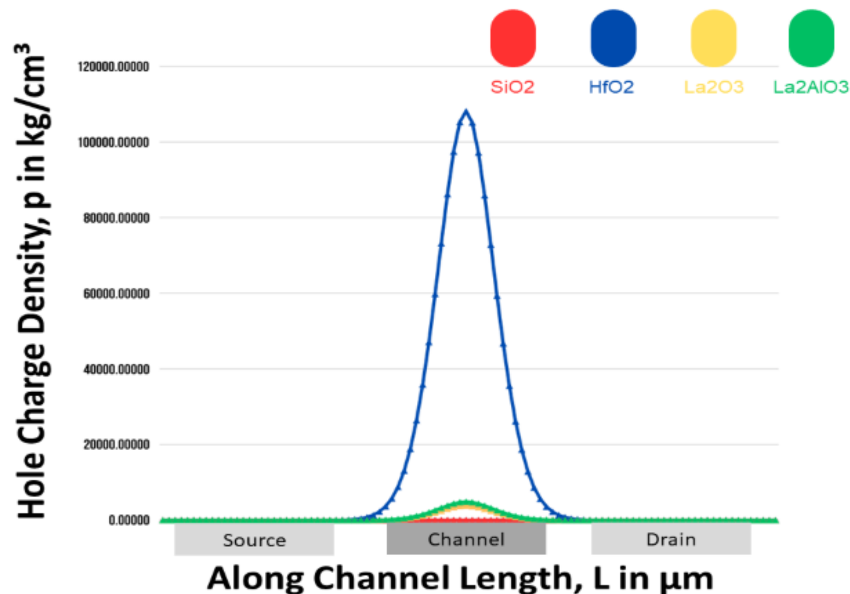

Figure 2: Hole Charge Density for HK materials HfO_2, La_2O_3 and $LaAlO_3$ and MG material as GaAs in comparison to SiO_2

The Seybold Report
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

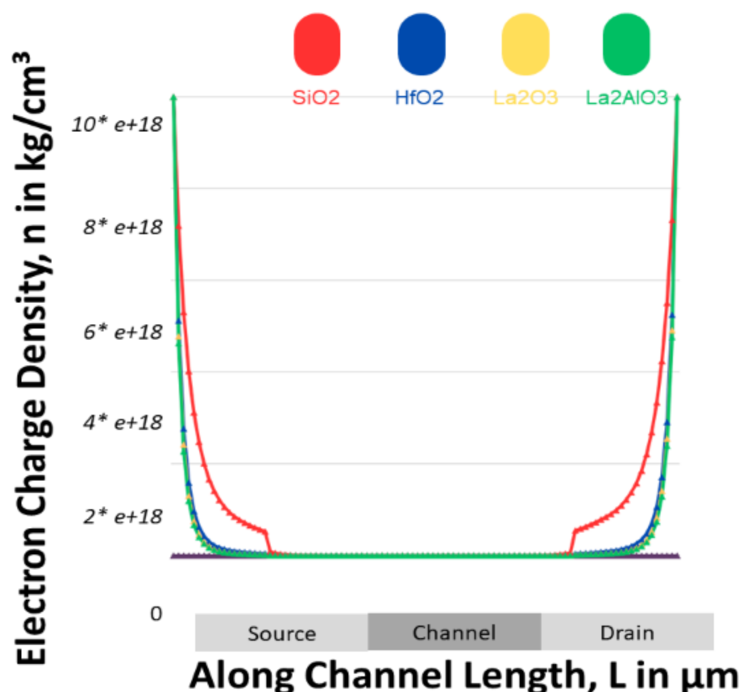

Figure 3: Electron Charge Density for HK materials HfO_2, La_2O_3 and $LaAlO_3$ and MG material as GaAs in comparison to SiO_2

Among the materials shown in Figures-2 and Figure-3, HfO_2 has the greatest density of hole charges, as seen by a prominent peak suggesting rapid hole accumulation. La_2O_3 and $LaAlO_3$ exhibit modest peaks, indicating a well-balanced rate of hole accumulation suitable for applications that need intermediate performance. SiO_2 has the lowest charge density, which means that holes develop slowly and reliably. This property makes it appropriate for applications requiring long-term stability. The electron charge density graph demonstrates that HfO_2 has the greatest density once again, as seen by a distinct peak, demonstrating effective electron accumulation. La_2O_3 and $LaAlO_3$ have low peaks, indicating their viability for applications that need equilibrated electron buildup. SiO_2 has the lowest electron density, suggesting that electrons accumulate steadily and continuously. This characteristic might be advantageous for applications that need low electron reactivity.

3.2 Electric Field Distribution

The distribution of electric fields in a semiconductor material has a significant impact on carrier mobility and device performance. Improving the electric field may boost carrier mobility and hence improve device performance. However, it is critical to understand that this increase in electric field may result in material breakdown or damage. On the other hand, reducing the electric field is safer for the material but may limit carrier mobility. High electric field materials are often employed in high-speed and high-frequency devices that need quick carrier transport, while low electric field materials are better suited for low-power, long-lasting devices.

The Seybold Report
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

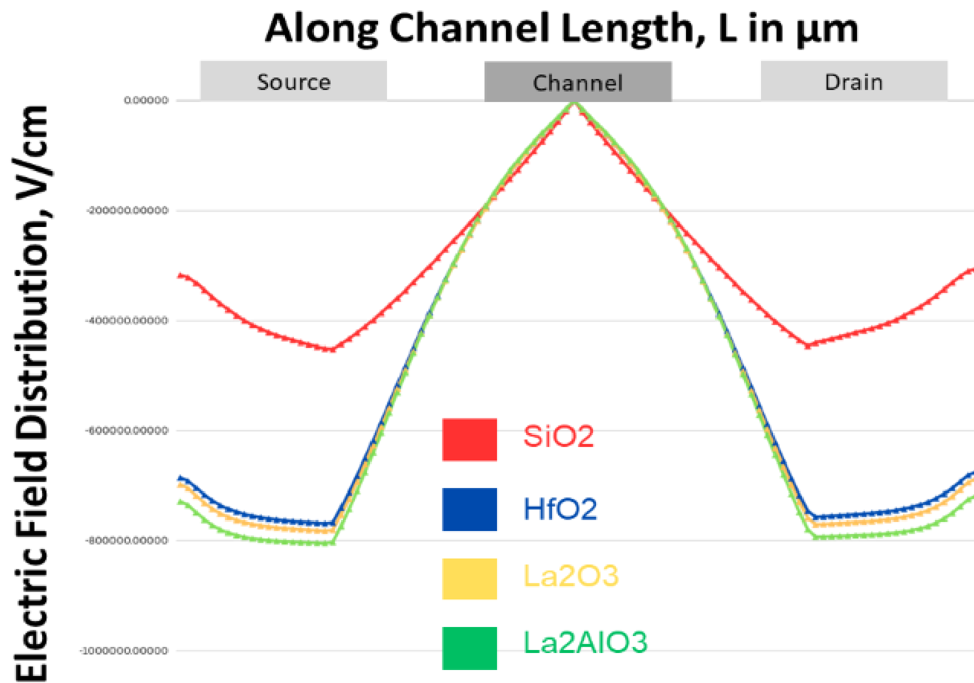

Figure 4: Electric Field Distribution for HK materials HfO_2, La_2O_3 and $LaAlO_3$ and MG material as GaAs in comparison to SiO_2

The electrical field distribution Figure-4 demonstrates that HfO_2 has the greatest peak electric field, suggesting that it is appropriate for high-field applications. La_2O_3 and $LaAlO_3$ have small field distributions, making them ideal for intermediate applications. SiO_2 has the best electric field distribution, but it is restricted by the larger electric field distribution at the source-drain ends caused by increased charge injection when compared to HfO_2, La_2O_3, and $LaAlO_3$.

3.3 Electro Static Potential

The voltage distribution within a semiconductor has a significant impact on carrier movement and device behavior since it is directly tied to the electrostatic potential. A higher electrostatic potential may result in more significant carrier movement, thereby improving device performance, while a lower potential may diminish carrier movement, reducing device efficiency. High-speed transistors, for example, depend substantially on electro-statically charged materials. Materials with lower potential are more suitable for applications that need stability and low power consumption. The electrostatic potential illustrated in Figure-5 shows that HfO_2, La_2O_3, and $LaAlO_3$ have the highest potential. The depth of each curve shows the magnitude of the electrostatic potential inside the channel area. SiO_2 has the lowest potential, making it ideal for applications that need a low electrostatic potential. According to the trend, HfO_2, La_2O_3, and $LaAlO_3$ are more suited to high-potential applications than SiO_2.

The Seybold Report
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

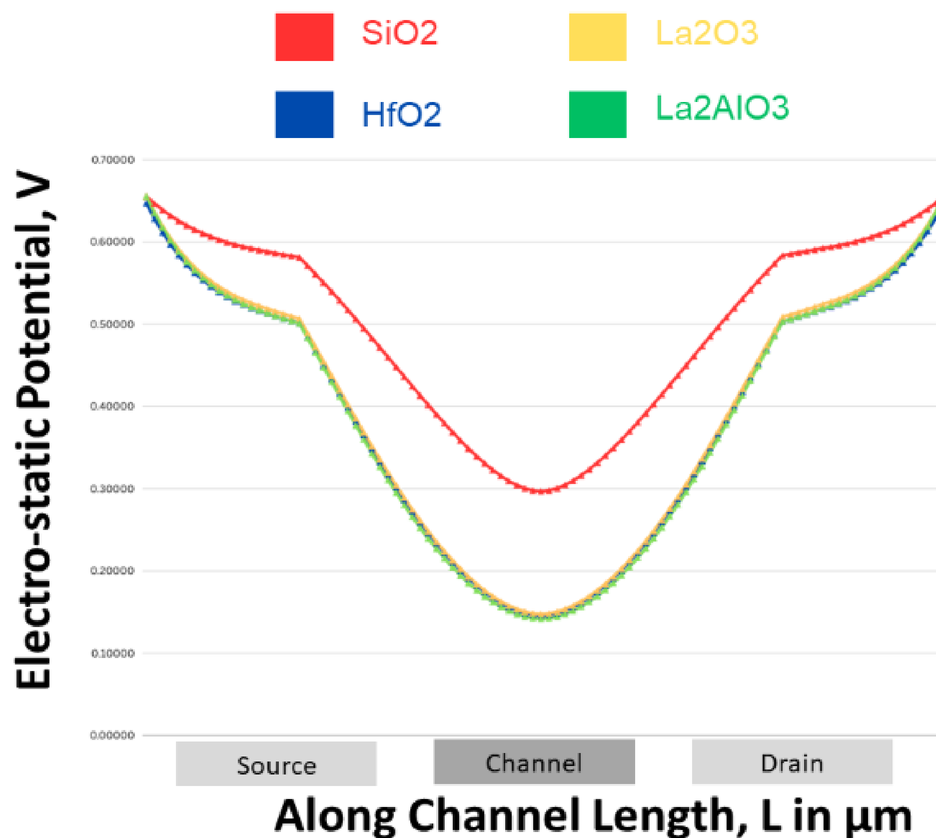

Figure 5: Electro static Potential for HK materials HfO_2, La_2O_3 and $LaAlO_3$ and MG material as GaAs in comparison to SiO_2

3.4 I-V Characteristics

I-V factors affect a material's conductivity and response to applied voltage. Current values may be used to assess conductivity and performance in conducting devices. Higher levels often indicate more conductivity, whilst lower values may be better suitable for insulating reasons. High current materials are essential for powering and boosting performance in applications requiring high power and speed, such as power transistors and amplifiers. Low current materials are utilized when insulation or restricted conductivity are needed. This increases stability and lowers power consumption. A device's threshold voltage (V_{th}) is defined as the point at which the drain current significantly rises. HfO_2, La_2O_3, and $LaAlO_3$ have lower threshold voltages than SiO_2, resulting in an earlier rise in drain current. HfO_2, La_2O_3, and $LaAlO_3$ have higher drain currents than SiO_2 over the threshold voltage. The steeper slopes illustrated in Figure-6 indicate better on-state performance, meaning that devices with high-k dielectrics can sustain higher driving currents. In the case of SiO_2, the threshold voltage is higher and the drain current rises less sharply, indicating less effective gate control and lower drive current capability. HfO_2, La_2O_3, and $LaAlO_3$ have lower threshold voltages and steeper rises in drain current, indicating improved gate control and drive current capabilities. This is

ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

consistent with the high dielectric constant, which increases gate capacitance and control. Furthermore, $LaAlO_3$ provides a greater drain current than HfO_2 and La_2O_3.

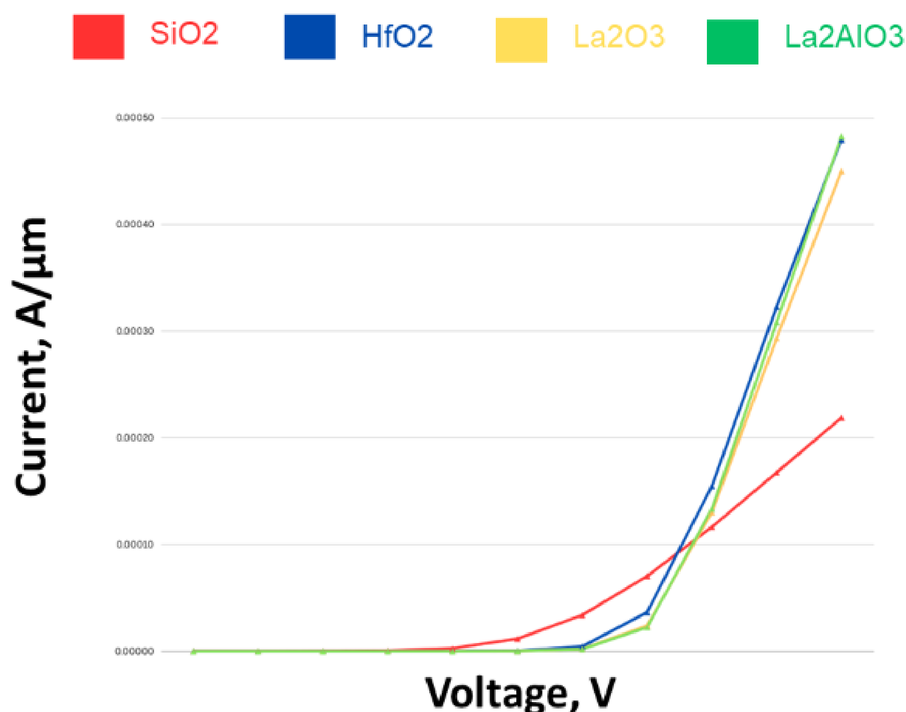

Figure 6: I-V Characteristics for HK materials HfO_2, La_2O_3 and $LaAlO_3$ and MG material as GaAs in comparison to SiO_2

3.5 Subthreshold Slope (SS)

The subthreshold swing evaluates a transistor's efficiency in transitioning from off to ON state. SS values may be used to determine the efficiency of switching in a device. Higher values indicate less efficient switching, requiring more voltage to turn the item on. Lower SS values, on the other hand, indicate more efficient switching, allowing the device to be turned on with less voltage. Devices with low SS are advantageous for low-power applications because to their energy economy while transitioning between states. Devices with high SS may use more power and generate more heat, rendering them unsuitable for power-sensitive applications. When looking at the subthreshold swing in Figure-7(a), it is evident that HfO_2 has the steepest slope, suggesting that it is less effective in terms of subthreshold swing. La_2O_3 and $LaAlO_3$ have mild slopes, indicating more efficiency than HfO_2. SiO_2 has the steepest slope, suggesting great efficiency in subthreshold swing, rendering it unsuitable for low-power applications.

3.6 Threshold Voltage (Vth)

Threshold voltage V_{th} is crucial to semiconductor device operation, especially field effect transistors (FETs). The threshold voltage is the lowest gate voltage necessary to establish a conductive connection between the source and drain terminals. The threshold voltage has a

The Seybold REPORT
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

substantial influence on transistor performance since it controls the transistor's switching characteristics. When the threshold voltage is raised, the transistor needs more voltage to activate. These qualities may result in slower switching rates and lower current flow, which may be advantageous in applications that need low power consumption and excellent noise margins. However, very high threshold voltages may impair the device's responsiveness and efficiency in high-speed applications. As illustrated in Figure-7 (b), when the threshold voltage lowers, the transistor may operate at a lower voltage. This performance boost results in quicker switching and better current driving capabilities. This is ideal for applications requiring high speed and performance. However, excessively low threshold voltages might result in higher leakage currents and power consumption while the device is not in use, which is undesirable in low-power environments. An optimal threshold voltage is crucial for achieving a balance between performance and power consumption in semiconductor devices. Materials like HfO_2, La_2O_3, and $LaAlO_3$ are ideal for applications requiring consistent and predictable performance because they can maintain a stable threshold voltage under changing conditions. SiO_2 may not be the ideal choice for certain applications due to a significant drop in threshold voltage. However, this propensity may be mitigated by addressing certain conditions. Understanding and controlling the threshold voltage is essential for creating high-performance, dependable semiconductor devices.

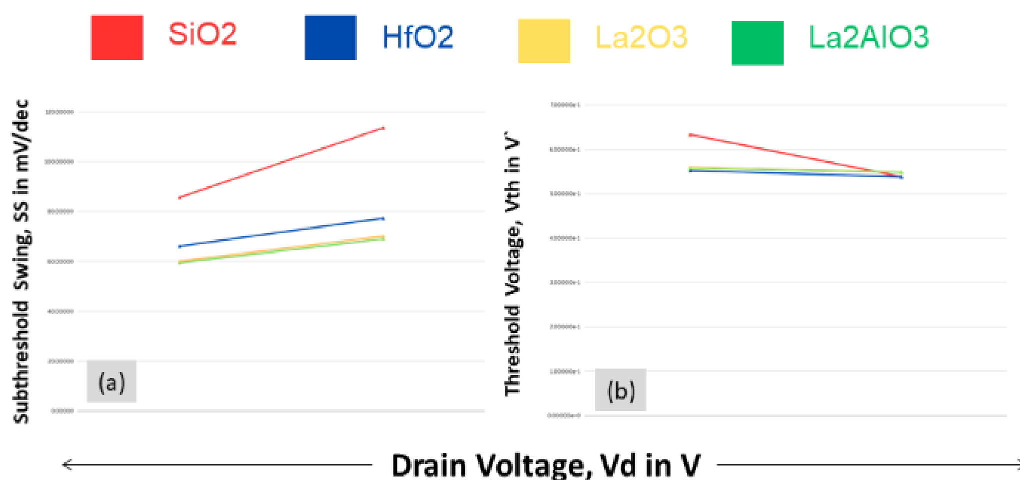

Figure 7: (a) SS, (b) V_{th} for HK materials HfO_2, La_2O_3 and $LaAlO_3$ and MG material as GaAs in comparison to SiO_2

3.7 Transconductance (gm)

Transconductance describes how a transistor's output current changes in response to variations in the input voltage. A higher transconductance implies stronger amplification and increased gain in the transistor, while a lower transconductance indicates poor amplification and lowered gain. Amplifiers and high-frequency applications need materials with high transconductance levels. These materials are crucial for achieving high gain and responsiveness. Materials with low transconductance may be employed in applications that need signal stability and lowest

The Seybold REPORT
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

gain, resulting in consistent performance and lower power consumption. The transconductance graph from Figure-8 reveals that $LaAlO_3$ has the highest transconductance, suggesting that it is ideal for high-performance applications. La_2O_3 and HfO_2 have strong transconductance, making them suitable for applications requiring balanced performance. SiO_2 has the lowest transconductance, making it suitable for situations where high transconductance is not an important issue.

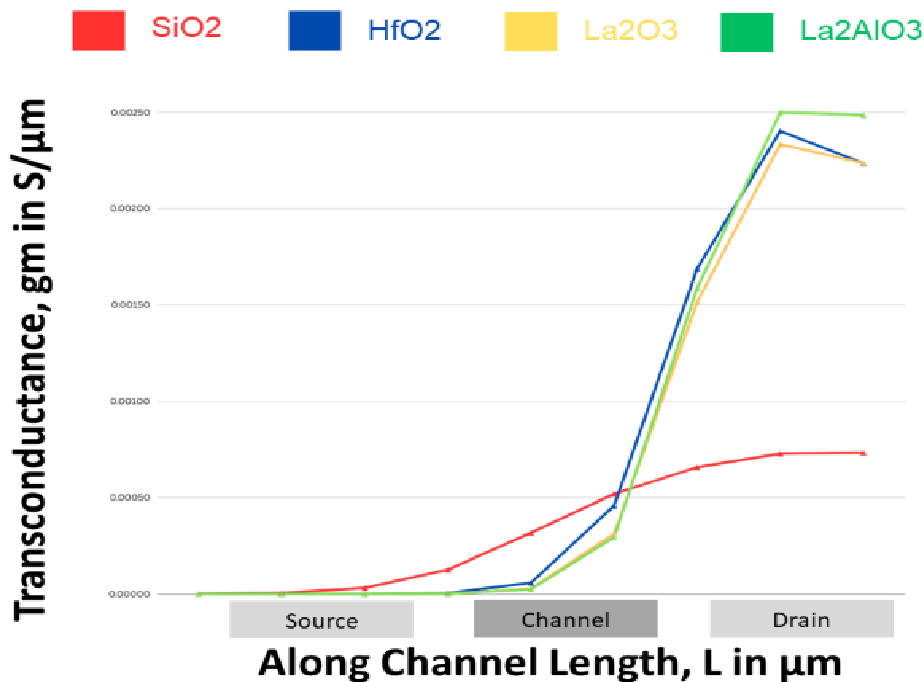

Figure 8: Transconductance for HK materials HfO_2, La_2O_3 and $LaAlO_3$ and MG material as GaAs in comparison to SiO_2

3.9 Drain Induced Barrier Lowering (DIBL)

DIBL is a phenomenon in MOSFETs in which the threshold voltage falls as the drain voltage increases. Higher DIBL values indicate higher short-channel effects, which may cause a reduction in threshold voltage and possibly unstable device behavior. Lower DIBL values imply greater management of these effects, resulting in a more stable threshold voltage. Devices with low DIBL are best suited for applications that need both high performance and low power consumption. This is due to their ability to stay consistent and predictable. Excessive DIBL may result in leakage currents and device failures, particularly in cutting-edge, small technologies. Figure-9 demonstrates that SiO_2 has the highest DIBL values, indicating sensitivity to short-channel effects. La_2O_3 and $LaAlO_3$ had lower DIBL values, suggesting that they control short-channel effects more effectively than HfO_2. $LaAlO_3$ has excellent control over short-channel effects, producing the lowest DIBL values. This characteristic makes it perfect for applications that demand precise control over this parameter.

The Seybold Report
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

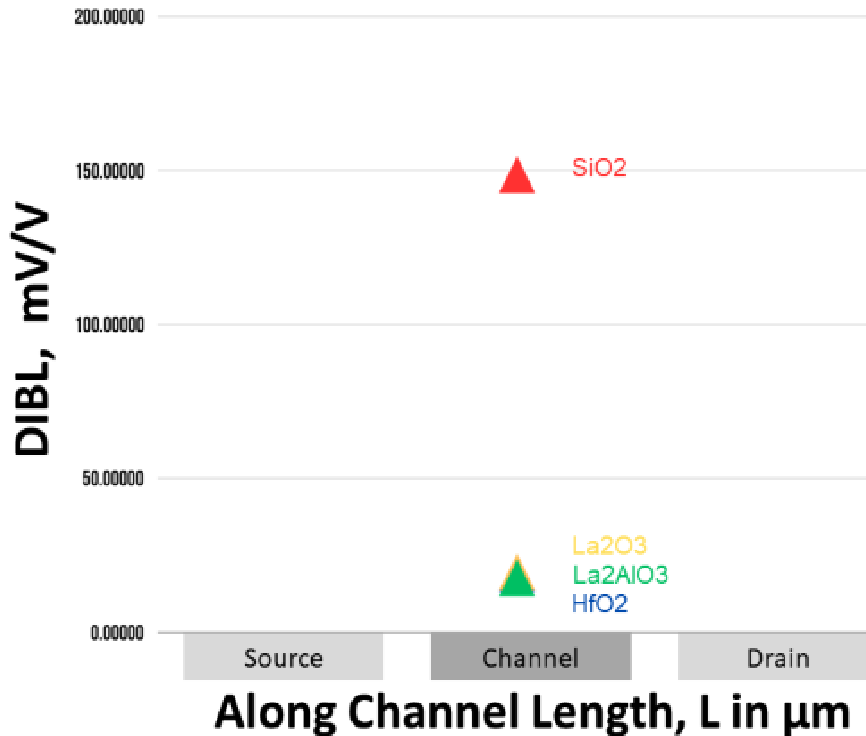

Figure 9: DIBL for HK Materials HfO_2, La_2O_3 and $LaAlO_3$ and MG Material as GaAs in Comparison to SiO_2

3.9 Transconductance Sensitivity (Sgm).

Transconductance (g_m) in FinFET devices is a fundamental property that measures the device ability to control the drain current (I_d(sat) or I_{ON}) using the gate voltage (V_{gs}). This feature is crucial for increasing device performance, especially in analog and RF applications. The transconductance of a FinFET is affected by the physical size of the fin and gate, as well as the gate oxide capacitance, carrier mobility, and threshold voltage. The transconductance is often expressed mathematically by the following equation (1).

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \quad (1)$$

The transconductance sensitivity S_{gm} in mS/k is given by equation (2)

$$S_{gm} = \frac{dg_m}{dT} \text{ in mS/k} \quad (2)$$

From Figure-10, it is evident that the transconductance sensitivity of the FinFET nanosensor is strongly temperature dependent, diminishing as the temperature rises. Moreover, the sensitivity of the FinFET device remains consistent over the temperature range, demonstrating that it is less sensitive to temperature fluctuations than the nano-sensor. The FinFET nanosensor has a

The Seybold Report
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

wider sensitivity range (mS/°C), making it more suitable for applications requiring high sensitivity at low temperatures. The FinFET device offers a moderate and consistent sensitivity (mV/°C), which may be advantageous for applications requiring consistent performance across a wide temperature range. The graph compares the temperature sensitivity of FinFET nanosensors to conventional FinFET devices. At low temperatures, the FinFET nano-sensor is very sensitive, but its sensitivity decreases significantly as temperature increases. In contrast, the FinFET technology maintains continuous sensitivity across a broad temperature range. This information is crucial for selecting the appropriate FinFET type based on the application's specific temperature requirements.

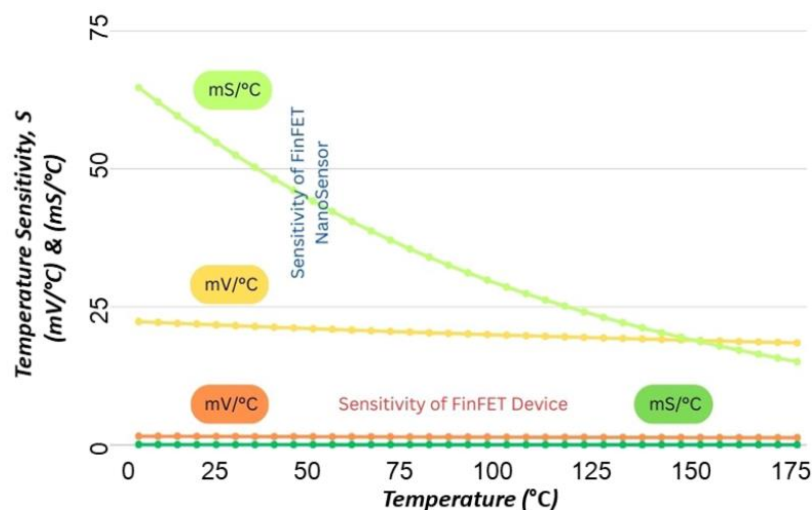

Figure 10: FinFET Nanosensor's temperature Sensitivity, S using voltage and transconductance based approaches in comparison to the FinFET's device sensitivity

3.10 Seebeck Coefficient (S)

The Seebeck coefficient (S) is a measurement of the thermoelectric voltage generated by a temperature difference across a material. It specifies the kind of charge carrier and the direction in which they travel inside the material when subjected to a temperature difference. The Seebeck coefficient in n-type FinFET devices is often negative, which may be explained by the nature of charge carriers and the thermoelectric effect in semiconductors. In n-type semiconductors, electrons constitute the majority of charge carriers. When a temperature gradient is applied, electrons go from the hot side (higher energy) to the cold side (lower energy). Because electrons are negatively charged, their travel causes a negative voltage difference. Because electrons are traveling towards the colder region, conventional current (measured in terms of positive charge flow) seems to flow in the opposite direction of electron movement. This yields a negative Seebeck coefficient.

The simulation findings reveal a high saw beck coefficient of larger than -250 $\mu V/K$ at T=275k, which lowers further to -378 $\mu V/K$ at T=450k. A high Seebeck coefficient in temperature sensors may enhance sensitivity, making S > -250 $\mu V/K$ a useful value for reliable temperature

The Seybold Report
ISSN 1533-9211
DOI: 10.5281/zenodo.13283086

measurement applications. A higher Seebeck coefficient in thermoelectric generators may improve efficiency, but it must be balanced against the material's ability to conduct electricity and manage heat.

IV. CONCLUSION AND FUTURE WORK

In this work, the performance metrics of a 7nm FinFET device employing high-k (HK) dielectric oxide materials with dielectric constants (k) of 24, 25, and 30, as well as Gallium Arsenide (GaAs) as the metal gate material is examined. Our research shows that HK dielectric materials, such as Hafnium Oxide (HfO_2), Lanthanum Oxide (La_2O_3), and Lanthanum Aluminum Oxide ($LaAlO_3$), considerably enhance FinFET device performance over standard SiO_2. Key performance parameters such as saturation drain current (Id(sat)), electric field distribution, threshold voltage (Vth), transconductance (gm), Drain Induced Barrier Lowering (DIBL), and subthreshold swing (SS) all demonstrate significant improvements. High-k dielectrics provide larger electron and hole charge densities, better electric field dispersion, and increased electrostatic potential, making them ideal for high-performance nanoelectronics applications. Additionally the studied voltage sensitivity was found to be 23mV/°C with a transconductance sensitivity of 66mS/°C and see beck coefficient of $S > -250\ \mu V/K$. This research indicates that HK dielectrics are better alternatives to traditional SiO_2 in the development of breakthrough FinFET technology.

Future research will concentrate on improving the integration of high-k dielectric materials in FinFET architectures to improve their performance and reliability. Specific areas of interest are: Thermal stability, scaling down, material innovations, device variation, and advanced modeling methodologies.

References

1) S. K.Saha, *FinFET Devices for VLSI Circuits and Systems*, vol. 5, no. 1. 2021.

2) B. S. Shim, W. Chen, C. Doty, C. Xu, and N. A. Kotov, “Smart Electronic Yarns and Wearable Fabrics for Human Biomonitoring made by Carbon Nanotube Coating with Polyelectrolytes,” 2008.

3) M. S. Alqahtani *et al.*, “Forecasting the Post-Pandemic Effects of the SARS-CoV-2 Virus Using the Bullwhip Phenomenon Alongside Use of Nanosensors for Disease Containment and Cure,” *Mater. 2022, Vol. 15, Page 5078*, vol. 15, no. 14, p. 5078, Jul. 2022, doi: 10.3390/MA15145078.

4) A. M. Mayet *et al.*, “Application of Nondestructive Techniques to Investigate Dissolvable Amorphous Metal Tungsten Nitride for Transient Electronics and Devices,” *Electron. 2022, Vol. 11, Page 3284*, vol. 11, no. 20, p. 3284, Oct. 2022, doi: 10.3390/ELECTRONICS11203284.

5) A. P. Jacob, R. Xie, M. G. Sung, L. Liebmann, R. T. P. Lee, and B. Taylor, “Scaling Challenges for Advanced CMOS Devices,” *Scaling Integr. High-Speed Electron. Optomech. Syst.*, pp. 1–76, 2017, doi: 10.1142/9789813225404_0001.

6) D. Yllmaz *et al.*, “DC and RF performance of lateral AlGaN/GaN FinFET with ultrathin gate dielectric,” *Semicond. Sci. Technol.*, vol. 37, no. 8, 2022, doi: 10.1088/1361-6641/ac7818.

7) V. Narendar and R. A. Mishra, “Analytical modeling and simulation of multigate FinFET devices and the impact of high-k dielectrics on short channel effects (SCEs),” *Superlattices Microstruct.*, vol. 85, pp. 357–369, 2015, doi: 10.1016/j.spmi.2015.06.004.

DOI: 10.5281/zenodo.13283086

8) D. Ryu, M. Kim, J. Yu, S. Kim, J. H. Lee, and B. G. Park, "Investigation of Sidewall High-k Interfacial Layer Effect in Gate-All-Around Structure," *IEEE Trans. Electron Devices*, vol. 67, no. 4, pp. 1859–1863, Apr. 2020, doi: 10.1109/TED.2020.2975255.

9) M. A. Muqeet, "DESIGN Of 7nm Finfet With High-K Dielectric Oxide And Metal Gate (Hk- Mg) Using Ashby ' S Ma Terial Selection (Ams) Approach Graphical Abstract : FinFET Device utilizing HK-MG using AMS," *J. Tianjin Univ. Sci. Technol.*, vol. 57, no. 02, pp. 204–218, 2024.

10) C. Park and I. Yun, "Optimization of self-heating driven leakage current proper-ties of gate-all-around field-effect transistors using neural network modeling and genetic algorithm," *Electron.*, vol. 10, no. 21, Nov. 2021, doi: 10.3390/ELECTRONICS10212570.

11) K. A. Gupta, D. K. Anvekar, and V. V., "Modeling of Short Channel MOSFET Devices and Analysis of Design Aspects for Power Optimisation," *Int. J. Model. Optim.*, vol. 3, no. 3, pp. 266–271, 2013, doi: 10.7763/ijmo.2013.v3.279.

12) M. A. Muqeet, "Analytical Modeling And Simulation Of A 7nm Hk-Mg Finfets Performance Investigation In Terms Of Improved Sensitivity For Temperature Nanosensing Applications," no. Ic, pp. 12–28, 2024, doi: 10.5281/zenodo.10803842.

13) H. T. AlAriqi, W. A. Jabbar, Y. Hashim, and H. Bin Manap, "Channel length-based comparative analysis of temperature and electrical characteristics for SiNWT and GeNWT," *Int. J. Comput. Digit. Syst.*, vol. 9, no. 1, pp. 87–95, 2020, doi: 10.12785/IJCDS/090109.

14) Y. Atalla, Y. Hashim, A. N. Abd Ghafar, and W. A. Jabbar, "A temperature characterization of (Si-FinFET) based on channel oxide thickness," *Telkomnika (Telecommunication Comput. Electron. Control.*, vol. 17, no. 5, pp. 2475–2480, 2019, doi: 10.12928/TELKOMNIKA.v17i5.11798.

15) M. A. Muqeet, "Design Of 7nm Finfet With High-K Dielectric Oxide And Metal Gate (Hk- Mg) Using Ashby ' S Ma Terial Selection (Ams) Approach Graphical Abstract : FinFET Device utilizing HK-MG using AMS," *J. Tianjin Univ. Sci. Technol.*, vol. 57, no. 02, pp. 204–218, 2024, doi: 10.5281/zenodo.10690824.

16) R. Saha, B. Bhowmick, and S. Baishya, "Deep insights into electrical parameters due to metal gate WFV for different gate oxide thickness in Si step FinFET," *Micro Nano Lett.*, vol. 14, no. 4, pp. 384–388, Apr. 2019, doi: 10.1049/MNL.2018.5220.

17) J. Westlinder *et al.*, "Investigation of Novel Metal Gate and High-κ Dielectric Materials for CMOS Technologies," 2004.

18) B. Raj, A. K. Saxena, and S. Dasgupta, "Quantum inversion charge and drain current analysis for double gate FinFET device: Analytical modeling and TCAD simulation approach," *Proc. - UKSim 4th Eur. Model. Symp. Comput. Model. Simulation, EMS2010*, pp. 526–530, 2010, doi: 10.1109/EMS.2010.93.

19) S. S. Chopade and D. V. Padole, "TCAD Simulation and Analysis of Drain Current and Threshold Voltage in Single Fin and Multi-Fin FinFET," *Indian J. Sci. Technol.*, vol. 10, no. 11, pp. 1–6, 2017, doi: 10.17485/ijst/2017/v10i11/93062.